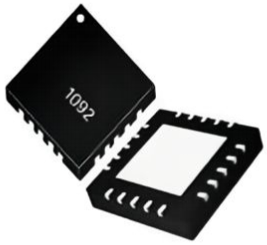
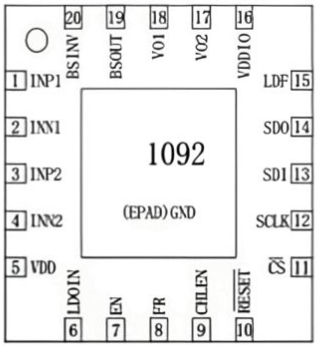
# Low-Noise 1-, 2-Channel Front-End Chip for ECG Biopotential Measurements

**Features**

- ♦ Single/Dual-channel low-noise analog front-end;
- ♦ Supply current: ~140 μA (1-channel);
  ~210 μA (2-channel);
- ♦ Shut down mode: <0.1 μA;
- ♦ Low input-referred noise: ~1 $\mu V_{rms}$;
- ♦ Common-mode rejection ratio: ~100 dB (DC-100 Hz);
- ♦ Single supply operation: 2 V to 3.6 V;
- ♦ Digital IO level: 1.8 V to 3.6 V;
- ♦ Programmable gain: 360 to 2720;
- ♦ Built-in filter bandwidth: 0.05 to 200 Hz;
- ♦ Built-in reference drive amplifier;
- ♦ Built-in SPI-compatible serial interface;
- ♦ Supports baseline fast restoring;
- ♦ Supports DC-coupled input;
- ♦ Supports dry-electrode input;
- ♦ ±4 kV HBM ESD rating;
- ♦ 3mm*3mm QFN-20 package;





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## General Description

The FS1091/FS1092 is an integrated single/dual-channel signal conditioning front-end for EEG and other weak biopotential measurements. The FS1091/FS1092 is designed to extract, amplify, and filter small biopotential (μV level) signals in the presence of noisy conditions. It incorporates programmable gain amplifiers (PGAs), filters, references, oscillators, digital serial peripheral interface (SPI), bias drive circuitry, and high-precision low-dropout regulator (LDO). With high-level integration and exceptional performance, the FS1091/FS1092 enables the development of scalable wearable devices at significantly reduced size, power, and overall cost.

The FS1091/FS1092 adopts a novel design of input impedance boosting. This feature allows dry electrodes, such as metal-plate electrodes and flexible fabric electrodes, to be used for weak biopotential recording. It dramatically enhances the user experience for wearable/portable application.

The FS1091/FS1092 has a flexible and wide-range gain (360 to 2720) configuration per channel through the onboard SPI to suit different types of applications.

The F S1091/FS1092 implements a high-pass filter for eliminating motion artifacts and the electrode half-cell potential. Additional low-pass filter is also incorporated to remove additional noise.

The FS1091/FS1092 includes a fast restore function that reduces the duration of the otherwise long settling tails of the high-pass filtering when an abrupt signal changes. This feature allows the FS1091/FS1092 to take valid measurements soon after connecting the electrodes to the subject.

The FS1091/FS1092 also with a built-in bias drive amplifier for driven lead applications, which helps improve the common-mode rejection of the line frequencies in the system and other interferences.

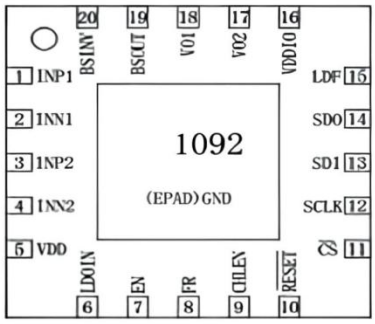
The FS1091/FS1092 is packaged in a 3 mm × 3 mm, 20-pin quad flat no-lead pack (QFN). Performance is specified from 0°C to 70°C and is operational from −40°C to +85°C.

## Applications

- **Wearable/Portable EEG Devices**
  - Brain-Computer Interface (BCI) devices, such as EEG helmets/headsets, etc.
  - Attention/Meditation training, Entertainment/Gaming peripherals.
- **Medical Equipment**
  - Multi-channel EEG equipment for EEG study/brain sciences;
  - Weak signal detection, such as fetal ECG, EMG, etc.

# 1. Pin Configuration and Description

## 1.1. Pin Configuration




## 1.2. Pin Description

| PIN NO. | NAME | FUNCTION | DESCRIPTION |
|---|---|---|---|
| 1 | INP1 (1) | Analog input | Differential analog positive input 1. |
| 2 | INN1 (1) | Analog input | Differential analog negative input 1. |
| 3 | INP2 (1)(2) | Analog input | Differential analog positive input 2. (2) |
| 4 | INN2 (1)(2) | Analog input | Differential analog negative input 2. (2) |
| 5 | VDD | Supply | Internal LDO output, 1.8V. |
| 6 | LDOIN | Supply | Internal LDO input. Chip power supply 2.0-3.6V. |
| 7 | EN | Digital input | Chip enable input. Active high. Connected to LDOIN or external logic high. Drive EN low to enter the low power shutdown mode. |
| 8 | FR | Digital input | Fast restore control, connect to LDF. Otherwise, drive it low if not used. |
| 9 | CHLEN (3) | Digital input | Signal channel enable input. Details see *SPI Registers* setting. |
| 10 | $\overline{\text{RESET}}$ | Digital input | System reset. Active low. Connect to $L_{DOIN}$, if not used. |
| 11 | $\overline{\text{CS}}$ | Digital input | SPI Chip select. Active low. |
| 12 | SCLK | Digital input | SPI master clock input. |
| 13 | SDI | Digital input | SPI data in. |
| 14 | SDO | Digital output | SPI data out. |
| 15 | LDF (4) | Digital output | Leads off detection output. Logic high for leads off and logic low for leads on. |
| 16 | VDDIO | Supply | Digital interface (SPI) IO level control input (typical 1.8/3.3 V). |
| 17 | VO2 (2) | Analog output | Signal channel 2 output. Connected to the input of an ADC. |
| 18 | VO1 | Analog output | Signal channel 1 output. Connected to the input of an ADC. |
| 19 | BSOUT | Analog output | Bias drive output. Connect to the driven electrode. |
| 20 | BSINV | Analog input | Bias drive inverting input. |
| EPAD | GND | Supply | Exposed pad. Chip supply ground. Connects to the global ground. |

*(1) connect to GND if not used.

*(2) available for dual-channel chip FS1092.

*(3) available for FS1092. To enable channel 1 and 2 simultaneously, configure both CHLEN and SPI **CHLnSET registers** are required.

*(4) only supports driven lead-off detection in strong power line interference conditions.

# 2. Electrical Characteristics

Minimum and maximum specifications apply from –40°C to +85°C. Typical specifications are at +25°C. LDOIN = 2 V to 3.6 V ± 10%, VDD = 1.8 V, VCM = VDD/2. All specifications are at VDD = 1.8 V, GND = 0 V, Gain=360, unless otherwise noted.

| Symbol | Parameter | Test Conditions/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Analog Input | | | | | | |
| | Differential Input Mode | | DC-coupling | | | |
| $V_d$ | Differential Input Range | | (VDD-0.15)/Gain | | | V |
| $V_{dc\_diff}$ | DC Differential Input Range | | -180 | | 180 | mV |
| $R_{in,\ amp}$ | DC Input Impedance | No pull-up or pull-down current source | | ~5 | | GΩ |
| | | Pull-up or pull-down current source | | 15 | | MΩ |
| Channel Performance | | | | | | |
| $A_v$ | Gain Setting | The first stage | 9,17 | | | |
| | | The second stage | 40, 60, 80, 120, 160 | | | |
| BW | Bandwidth | | 0.05 | | 200 | Hz |
| CMRR | Common-Mode Rejection Ratio | Vcm =0.9 V, Vc =0 V, f=DC to 100 Hz | | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | LDOIN = 2 V to 3.3 V | 85 | 105 | | dB |
| $V_n$ | Input-Referred Noise | f= 0.1 Hz to 220 Hz | | 1 | | $\mu V_{rms}$ |
| Right Leg Drive Circuitry | | | | | | |
| | Output Voltage Swing | | 0.1 | | VDD-0.1 | V |
| $R_{REF}$ | Load Resistor | Bias(reference electrode)driving | 10 | | 100 | kΩ |
| GDP | Gain Bandwidth Product | | | 10 | | kHz |
| Logic Interface | | | | | | |
| $V_{IH}$ | Input Voltage High | | 1.3 | | | V |
| $V_{IL}$ | Input Voltage Low | | | | 0.4 | V |
| $V_{OH}$ | Output Voltage High | | 0.8×VDDIO | | | V |
| $V_{OL}$ | Output Voltage Low | | | | 0.3 | V |
| System Specification | | | | | | |
| $L_{DOIN}$ | Supply Range | | 2.0 | 3.3 | 3.6 | V |
| $V_{LDO}$ | LDO Output Voltage | LDOIN=1.8V | | 1.79 | | V |
| | | LDOIN=3.3V | | 1.8 | | V |
| $V_{drop}$ | LDO drop-out Voltage | LDO output (PIN 5: VDD) | | 10 | 30 | mV |
| $I_{supply}$ | Supply Current | Single-channel, LDOIN=2 to 3.3V | | 140 | | μA |
| | | Dual-channel, LDOIN=2 to 3.3V | | 220 | | μA |
| $I_L$ | Load Current | LDO output (PIN 5: VDD) | | 10 | 30 | mA |
| $T_{st}$ | Startup Time | Supply voltage = 2 to 3.6 V | 60 | | 100 | μS |
| $I_{leak}$ | Shutdown Current | EN=Low | | 0.5 | | μA |
| $I_L$ | Load Current | LDO output (PIN 5: VDD) | | 10 | 30 | mA |
| C | Load Capacitor | LDO output (PIN 5: VDD) | 0.5 | | 4.7 | μF |
| $T_a$ | Operation Temperature | Normal mode | 0 | | +70 | °C |
| ESD | ESD Ratings | Human body model (HBM) | ±4 | | | kV |
| | | Charged device model (CDM) | | ±500 | | V |



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## 2.1. Absolute Maximum Ratings*

| Symbol | Parameter | Test Conditions | Value | Unit |
|---|---|---|---|---|
| LDOIN | Supply Voltage | $L_{DOIN}$ to GND | 1.8 to 3.7 | V |
| VDDIO | Digital Interface Logic Level | $V_{DDIO}$ to GND | 1.8 to 3.7 | V |
| $T_a$ | Operational Temperature | | -40 to +85 | °C |
| ESD | ESD Ratings | Human body model (HBM) | 8 | kV |
| | | Charged device model (CDM) | 1 | kV |

* Stresses at or above those listed under Absolute Maximum Ratings may, or will, cause permanent damage to the product. This is a stress rating only, and functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may degrade device performance and affect product reliability.

# 3. ESD Caution

ESD (Electrostatic Discharge) sensitive device.

Although this product features priority protection circuitry, damage may occur on devices subjected to high energy ESD or improper handling and installation procedures. ESD damage can range from subtle performance degradation to complete device failure. Therefore, appropriate ESD precautions should be taken to avoid performance degradation or loss of functionality, particularly for precision integrated circuits.

# 4. Theory of Operation

## 4.1. Architecture Overview

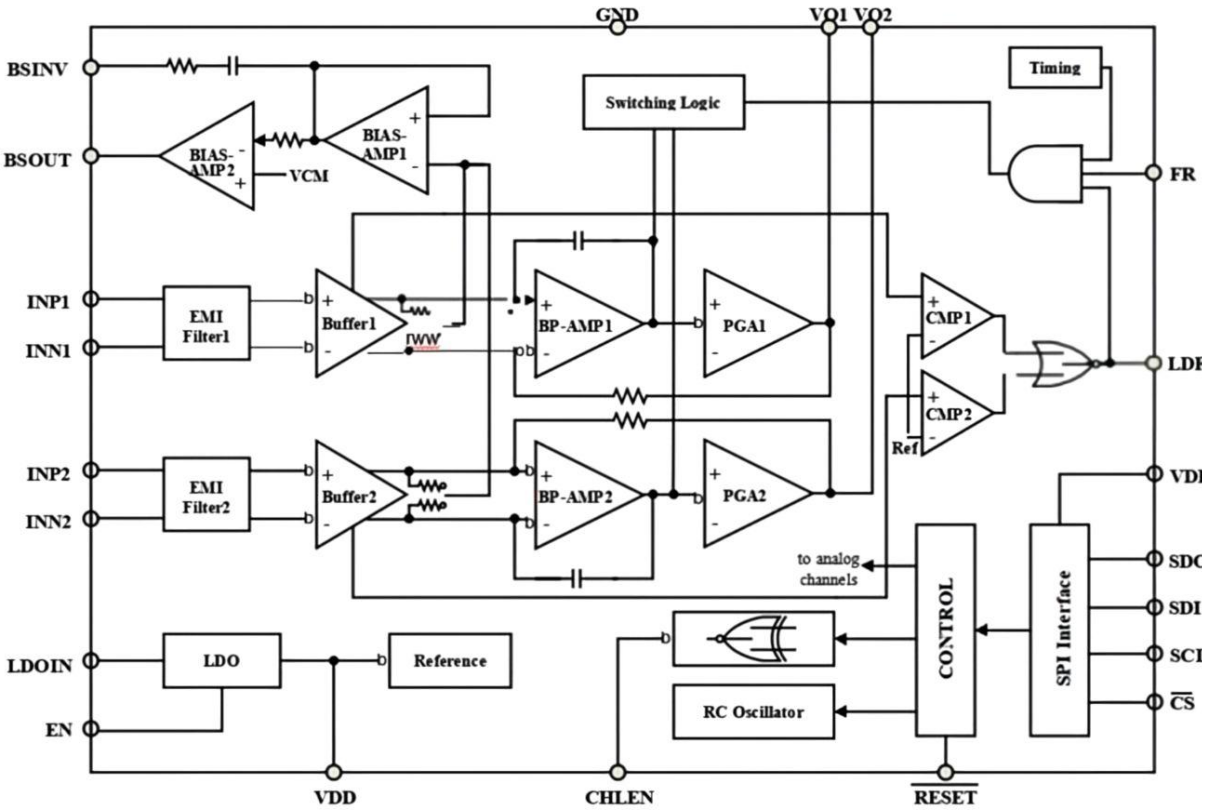


Figure 1. Function Block Diagram

The FS1091/FS1092 is an integrated single/dual-channel front end for signal conditioning of small biopotentials monitoring. Each channel consists of a buffer with high input impedance, a band-pass amplifier (BP -AMP), and a low-noise and programmable gain amplifier (PGA). The FS1091/ FS1092 contains a specialized band-pass amplifier with suitable bandwidth for low frequency biopotential and an optimized low noise amplifier with wide-range gain setting that can be configured by the serial peripheral interface (SPI). In addition, the FS1091/FS1092 includes leads off detection circuitry and an automatic fast restore circuitry that restores the signal shortly after leads are reconnected. To suppress undesired noise and interference, a bias drive amplifier (BIAS-AMP), high precision references and a low noise low dropout regulator (LDO) are also incorporated in this integrated circuit.

## 4.2. Signal Conditioning

The signal channel in the FS1091/FS1092 has a two-stage gain setting to achieve a large dynamic range for weak biosignals. Each stage gain can be programmed by the SPI register independently. The FS1091/FS1092 has high DC input impedance by means of an extinctive impedance isolation design skill. What' s more, this feature supports signal input from dry-contact electrodes in practical applications. The built-in BP-AMP amplifies the ECG signal while rejecting the DC offsets and electrode half-cell potential on the same stage. Consequently, DC offsets as large as 360 mV across the inputs will not saturate the signal channel. Meanwhile, the amplification of the biopotential and the rejection of the DC signal are possible with an indirect current feedback architecture, which reduces size and power compared with traditional implementations. After that, a signal with a large voltage

dynamic range can be obtained by the PGA through reasonable gain setting, which can be easily captured by an analog-to-digital converter (ADC) or an embedded ADC in a micro controller.

## 4.3. Analog Input

The FS1091/FS1092 analog input is fully differential. The differential input (INP-INN) can span between $\frac{VDD-0.15}{2}$ V. Generally, there are two different methods of driving the FS1091/FS1092 analog input: Single-Ended or Differential, as shown in Figure 2. Note that INP and INN are 180°C out-of-phase in the differential input method.

When the input is Single-Ended, the INN input is held at the common-mode voltage, preferably INP+INN at mid-supply. When the input is differential, the common-mode is given by V. For optimal performance, it is recommended that the FS1091/FS1092 be used in a **differential configuration.**


Sing-End Input Differential Input

Figure 2. Methods of Driving the FS1091/FS1092: Single-Ended or Differential.hat allows DC-coupling input for biopotential acquisitions.

## 4.4. Channel Gain Setting

The FS1091/FS1092 offers flexible gain with two-stage independent gain setting through an SPI interface for differential biopotential measurements. The channel gain can be chosen from one of ten settings (360, 540, 680, 720, 1020, 1080, 1360, 1440, 2040, and 2720), which can be set by writing to the CH1SET/CH2SET register. The details of the CH1SET and CH2SET registers are shown in the SPI Interface (SPI Register Definition) section.

The default gain setting of the FS1091/FS1092 is around 360. In practical application, keeping the gain in a reasonably low range helps with any motion artifacts picked up in band. To optimize the dynamic range of the system, the gain level is adjustable through the SPI registers, depending on the input signal amplitude (which may vary with electrode placement) and ADC input range.

## 4.5. Bias Drive Circuitry

The bias drive circuitry is used as a means to counter the common-mode interference in a biopotential measurement system as a result of power lines and other sources, including fluorescent lights. The basic principle is that the bias amplifier (BIAS-AMP) senses the common-mode signal that present at the device inputs, and forms a negative feedback loop by driving the subject with an inverted common-mode signal. The negative feedback loop restricts the common-mode variations to a narrow range.

As shown in Figure 3, the common-mode signal that is present across the inputs of the signal channel is derived from the BIAS-AMP1. It is then connected to the inverting input of BIAS-AMP2 through a resistor. An integrator can be built by connecting a capacitor between the BSINV and BSOUT terminals. A 1-nF capacitor is available in practical applications. This configuration results in good common-mode line rejection in a frequency range from 50 Hz to 60 Hz. Higher capacitor values may reduce the loop gain that is available for rejection and, consequently, increase the line noise. Lower capacitor values move the crossover frequency to higher frequencies,

allowing increased gain. The trade off is that with higher gain, the system can become unstable and saturate the output of the BIAS-AMP2.

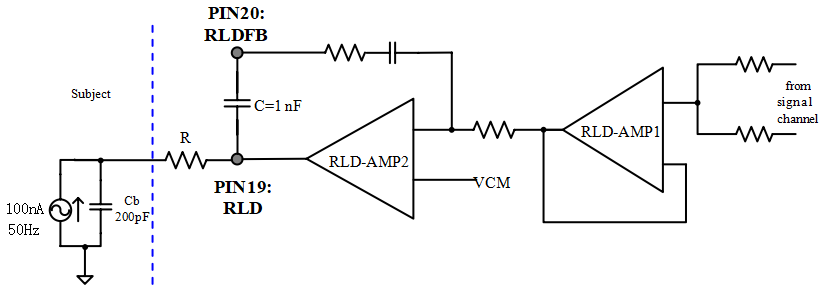


Figure 3. Typical Configuration of RLD Circuitry.

For absolute safety consideration, when using this RLD circuitry to drive an electrode, a resistor R in series with the output (PIN19: RLD) to limit the current to be less than around 20 μA is recommended. For example, if the supply used is 1.8 V, ensure that the resistor is greater than 100 kΩ to account for component and supply variations. It is important to point out that a large resistor R between the RLD output and the subject may degrade the interference rejection performance. Thus, the value of the resistor R can be used from 10 kΩ to 100 kΩ in battery-powered systems for general-purpose use.

## 4.6. Fast Restore Circuitry

The FS1091/FS1092 adopts a band-pass amplifier (BP-AMP). Due to the ultra-low cutoff frequency of the high -pass filtering characteristic, signals may require several seconds to settle. This settling time can result in a frustrating delay for the user after a step response: for example, when the electrodes are first connected. This fast restore control block, as shown in Figure 4, is implemented to reduce the large delay. The output of the signal channel is connected to a window comparator. Once a saturation condition at the output of the signal path is detected by the window comparator, which triggers a timing circuit. Thus, a low resistance loop path between the input and output of the BP-AMP will be created to deliver a quicker settling time. If, by the end of the timing, the saturation condition persists, the cycle repeats. Otherwise, the FS1091/FS1092 returns to its normal operation.

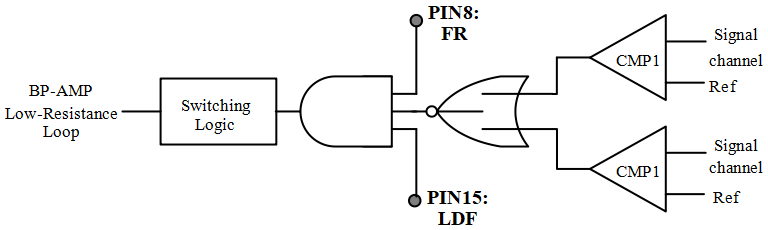


Figure 4. Fast Restore Circuitry.

The FS1091/FS1092 allows the user to select the input to trigger the timing switches of this fast restore function block: internal lead off detection output (PIN15: LDF) and external control signal (PIN8: FR). An external signal can be created by specified circuits and embedded programs in micro controllers (MCUs).

To disable fast restore, drive the FR pin low or tie it permanently to GND.

## 4.7. Power Supply Regulation

With a high-precision low dropout regulator (LDO), the FS1091/FS1092 is designed to be powered directly from a single supply voltage range from 1.8 V to 3.6 V. The output voltage of this LDO is 1.8 V (PIN5: VDD), which provides a precision supply voltage for internal circuits of the FS1091/FS1092.

To enhance the PSRR performance of the LDO, higher than 1.8 V single supply voltage is recommended to use. The FS1091/FS1092 can be driven by a single 3 V battery, such as the CR2025 or CR2032 type. It can also

operate from rechargeable Li-Ion batteries, but the designer must take into account that the voltage during a charge cycle may exceed the absolute maximum ratings of the FS1091/FS1092. To avoid damage to the device, use a power switch or a DC-DC buck device.

Benefit from the built-in low-noise LDO, an additional off-the-shelf high-precision LDO chip for analog circuits in the system solution is not required when this product is used for small biopotential measurements. It can help reduce the system size and power, as well as cost.

## 4.8. Channel ON/OFF Mode

The FS1091/FS1092 includes an enable pin (PIN7: EN) that allows channel/channels ON/OFF configuration. A logic low-level signal can be applied to this pin to switch to OFF mode, even when the supply is still on. Place EN to chip supply (PIN6: LDOIN) if not using this feature.

## 4.9. Shutdown Mode

The FS1091/FS1092 can work in shutdown mode, which further enhances the flexibility and ease of use in portable applications where power consumption is critical.

Driving the EN pin (PIN7: EN) as well as the VDDIO pin (PIN16: VDDIO) both low places the FS1091/FS1092 in shutdown mode and draws less than 0.1 μA of supply current, offering considerable power savings.

To enter normal operation, drive EN and VDDIO high. If not using this feature, permanently tie EN to chip supply (PIN6: LDOIN) and VDDIO to digital supply voltage.

Notice that all circuits in the FS1091/FS1092 will enter sleep mode during shutdown operation.

## 4.10. I/O Protection

All terminals of the FS1091/FS1092 are protected against ESD with specialized circuitry. The measured ESD rating for each pin of the FS1091/FS1092 is about ±4 kV for HBM mode, and ±500 V for CDM mode. In addition, the input structure allows DC overload conditions that are a diode drop above the positive supply and a diode drop below the negative supply. Voltages beyond the diode drop of the supplies cause the ESD diodes to conduct and enable current to flow through the diode. Therefore, it is necessary to ensure each of the inputs with limited voltage that does not exceed the supplies.

# 5. SPI Interface

## 5.1. I/O Description

The serial peripheral interface (SPI)-compatible serial interface consists of four signals: CS, SCLK, SDI, and SDO. The interface reads and writes registers and controls FS1091/FS1092 operation.

### 5.1.1. Chip Select (CS)

CS selects the FS1091/FS1092 for SPI communication. CS must remain low for the entire duration of the serial communication. After the serial communication is finished, always wait for four or more tCLK cycles before taking CS high. When CS is taken high, the serial interface is reset, SCLK and SDI are ignored, and SDO enters a high-impedance state.

### 5.1.2. Serial Clock (SCLK)

SCLK is the SPI serial clock. SCLK is used to shift commands in and shift data out from the device. The serial clock features a Schmitt triggered input and clocks data on the SDI and SDO pins into and out of the FS1091/FS1092. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally forcing a clock event. When shifting in commands with SCLK, make sure that the entire set of SCLKs is issued to the device. Failure to do so could result in the device serial interface being placed into an unknown state, requiring CS to be taken high to recover.

### 5.1.3. Data Input (SDI)

The data input pin (SDI) is used along with SCLK to communicate with the FS1091/FS1092 (opcode commands and register data). The device latches data on SDI on the SCLK falling edge.

### 5.1.4. Data Output (SDO)

The data output pin (SDO) is used with SCLK to read register data from the FS1091/FS1092. Data on SDO are shifted out on the SCLK rising edge. SDO goes to an available state when CS is low. In read data continuous mode (see the SPI Command Definitions section for more details), the SDO output line also indicates when new data are available. This feature can be used to minimize the number of connections between the device and the system controller.

## 5.2. Timing Characteristics

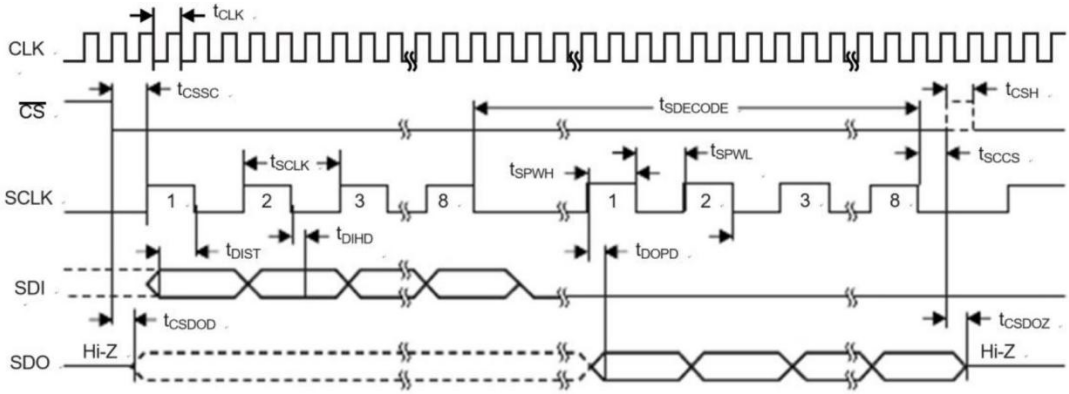


Figure 5. SPI Timing Diagram



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| Parameter | Description |
|---|---|
| $t_{CLK}$ | Master clock period |
| $t_{CSSC}$ | CS low to first SCLK, setup time |
| $t_{SCLK}$ | SCLK period |
| $t_{SPWHL}$ | SCLK pulse width, high and low |
| $t_{DIST}$ | SDI valid to SCLK falling edge: setup time |
| $t_{DIHD}$ | Valid SDI after SCLK falling edge: hold time |
| $t_{DOPD}$ | SCLK rising edge to SDO valid |
| $t_{CSH}$ | CS high pulse |
| $t_{CSDOD}$ | CS low to SDO driven |
| $t_{SCCS}$ | Eighth SCLK falling edge to CS high |
| $t_{SDECODE}$ | Command decode time |
| $t_{CSDOZ}$ | CS high to SDO Hi-Z |

## 5.3. SPI Command Definitions

The FS1091/FS1092 provides flexible configuration control. The opcode commands summarized in the following table control and configure the FS1091/FS1092 operation. The opcode commands are stand-alone, except for the register read and register write operations, which require a second command byte plus data. CS can be taken high or held low between opcode commands but must stay low for the entire command operation (especially for multi-byte commands). System opcode commands and the RDATA command are decoded by the FS1091/FS1092 on the seventh SCLK falling edge. The register read and write opcodes are decoded on the eighth SCLK falling edge. Be sure to follow SPI timing requirements when pulling CS high after issuing a command.

| Command | Description | Opcodes | Operand |
|---|---|---|---|
| RESET | Reset the device | 1111_1110(0xFE) | -- |
| RDATA | Read data by command; supports multiple read back. | 0000_0001(0x01) | -- |
| RREG | Read nnnn registers starting at address rrrr | 0001_rrrr(0x1x) | xxxx_nnnn |
| WREG | Write nnnn registers starting at address rrrr | 0010_rrrr(0x2x) | xxxx_nnnn |

(1) nnnn = number of registers to be read or written. For example, to read or write three registers, set nnnn = 0010.

(2) rrrr = starting register address for read and write opcodes.

### 5.3.1. RESET: Reset Registers to Default Values

This command resets and returns all register settings to the default values. There are no restrictions on the SCLK rate for this command, and it can be issued at any time. Avoid sending any commands during this time.

### 5.3.2. RDATA: Read Data

There is no restriction on the SCLK rate for this command, and there is no wait time needed for the subsequent commands or data retrieval SCLKs. To retrieve data from the device after the RDATA command is issued. The following figure shows the recommended way to use the RDATA command.

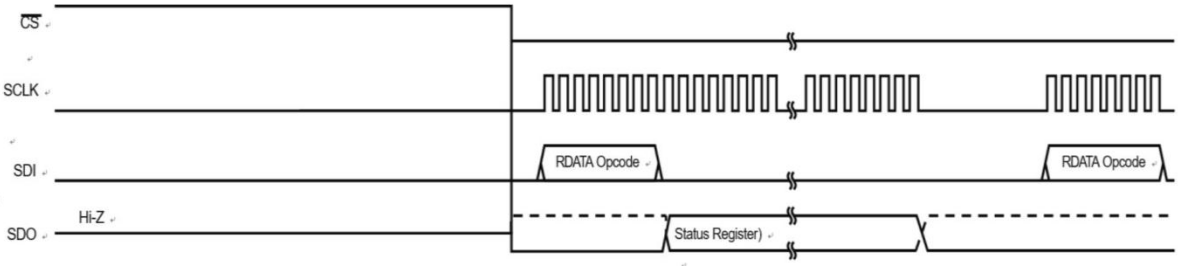


Figure 6. RDATA Usage

### 5.3.3. RREG: Read from Register

This opcode reads register data. The Register Read command is a two-byte opcode followed by the output of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to read.

First opcode byte: 0001 rrrr, where rrrr is the starting register address.

Second opcode byte: 000 nnnn, where nnnn is the number of registers to read.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in The following figure. The RREG command can be issued at any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the Serial Clock (SCLK) subsection of the SPI Interface section for more details. Note that CS must be low for the entire command.

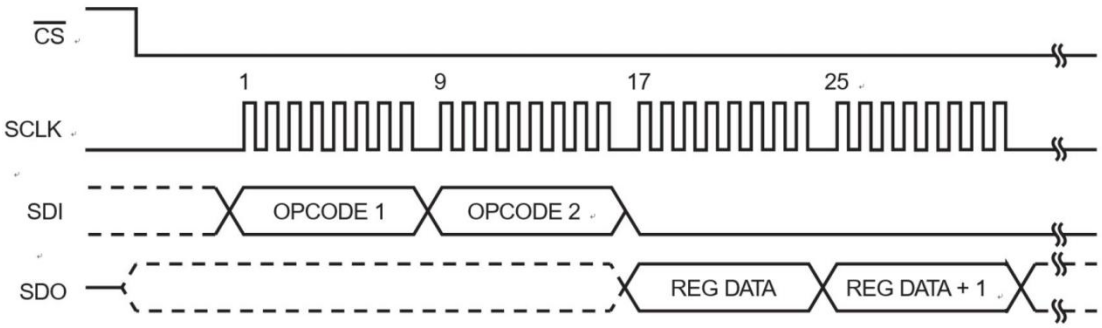


Figure 7. RREG Command Example: Read Two Registers Starting from Register 00h (CH1SET Register in FS1091/FS1092).

(OPCODE 1 = 0001 0000, OPCODE 2 = 0000 0001)

### 5.3.4. WREG: Write to Register

This opcode writes register data. The Register Write command is a two-byte opcode followed by the input of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to write.

First opcode byte: 0010 rrrr, where rrrr is the starting register address.

Second opcode byte: 0000 nnnn, where nnnn is the number of registers to write.

After the opcode bytes, the register data follows (in MSB-first format), as shown in the following figure. The WREG command can be issued at any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the Serial Clock (SCLK) subsection of the SPI Interface section for more details. Note that CS must be low for the entire command.

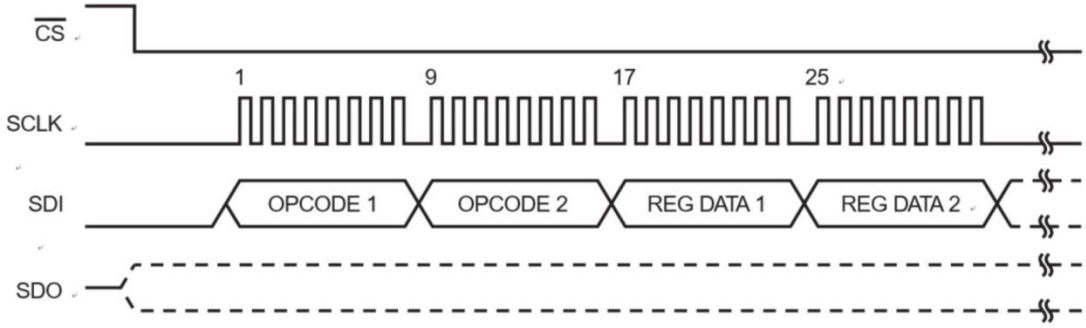


Figure 8. WREG Command Example: Write Two Registers Starting from 00h (CH1SET Register

(OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

## 5.4. SPI Register Definition

### 5.4.1. Register Assignment

| Address | Register | Default Value | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 00h | CH1SET | 0010_0000 | Reserved | Reserved | CHLPD | Gain2_2 | Gain2_1 | Gain2_0 | Gain1_1 | Gain1_0 |
| 01h | CH2SET | 0010_0000 | Reserved | Reserved | CHLPD | Gain2_2 | Gain2_1 | Gain2_0 | Gain1_1 | Gain1_0 |

### 5.4.2. User Register Description

#### 5.4.2.1. CH1SET: Channel 1 Settings (Address=0000, Default Value=0010_0000)

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | CHL1PD | Gain2_2 | Gain2_1 | Gain2_0 | Gain1_1 | Gain1_0 |
| Bit[7:6] | **Reserved** 00 (default). | | | | | | |
| Bit[5] (1) | **CHL1PD[1] together with PIN 9 (CHLEN): Channel Power Down and Power Up.**1(default);0.<br>**NOTE**(2) : CHL1PD **XOR CHLEN = 1,** Enable Channel 1;CHL1PD **XOR CHLEN = 0,** Shut Down Channel 1. | | | | | | |
| Bit[4:2] | **Gain2[2:0]: the second-stage gain setting of Channel 1** 000=40 (default);100=60;101=80;110=120;111=160. | | | | | | |
| Bit[1:0] | **Gain1[1:0]: the first-stage gain setting of Channel 1** 00=9 (default);10=7. | | | | | | |

#### 5.4.2.2. CH2SET: Channel 2 Settings (Address = 0001, Default Value = 0010_0000)

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | CHL2PD | Gain2_2 | Gain2_1 | Gain2_0 | Gain1_1 | Gain1_0 |
| Bit[7:6] | **Reserved** 00 (default). | | | | | | |
| Bit[5] (1) | **CHL2PD[1] together with PIN 9 (CHLEN): Channel Power Down and Power Up.**1(default);0.**NOTE(2) :**<br>CHL2PD **XNOR CHLEN = 1,** Enable Channel 2;CHL2PD **XNOR CHLEN = 0**, Shut Down Channel 2. | | | | | | |
| Bit[4:2] | **Gain2[2:0]: the second-stage gain setting of Channel 2** 000=40 (default);100=60;101=80;110=120;111=160. | | | | | | |
| Bit[1:0] | **Gain1[1:0]: the first-stage gain setting of Channel 2** 00=9 (default);10=17. | | | | | | |

*(1) available for dual-channel chip FS1092.

*(2) details see the following truth table for channel selection.



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## 5.5. Channel Selection Description

### 5.5.1. Channel 1

| CHL1PD | CHLEN | CHANNEL 1 | Logic Operation |
|---|---|---|---|
| 1 | 0 | ON | **XOR:** CHL1PD⊕CHLEN |
| 1 | 1 | OFF | |
| 0 | 0 | OFF | |
| 0 | 1 | ON | |

### 5.5.2. Channel 2

| CHL2PD | CHLEN | CHANNEL 2 | Logic Operation |
|---|---|---|---|
| 1 | 0 | OFF | **XNOR:** CHL2PD⊙CHLEN |
| 1 | 1 | ON | |
| 0 | 0 | ON | |
| 0 | 1 | OFF | |


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# 6. Application Information

As a case, the FS1091/FS1092 can be used to record small biopotentials with minimal distortion. In addition, space is at a premium for wearable device configuration. As shown in Figures 9 and 10, by using as few external components as possible, the application circuit based on the FS1091/FS1092 is optimized for size.

## 6.1. Application Circuits

There are two different types of circuit configuration according to the chip category. The circuits in Figure 9 and Figure 10 are designed for monitoring single-lead and dual-channel ECG, respectively.

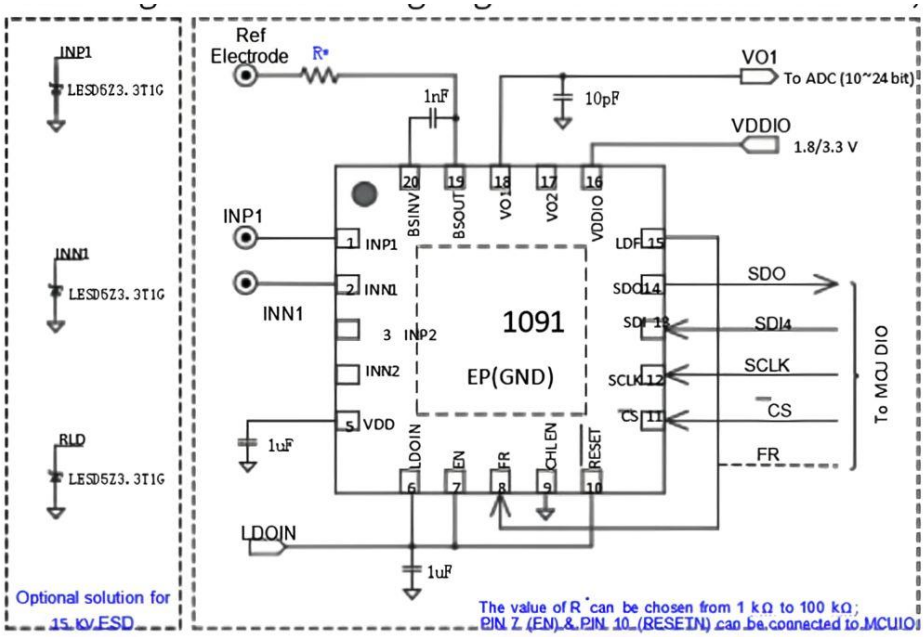


Figure 9. Signal-Channel Signal Conditioning with **3** Electrodes

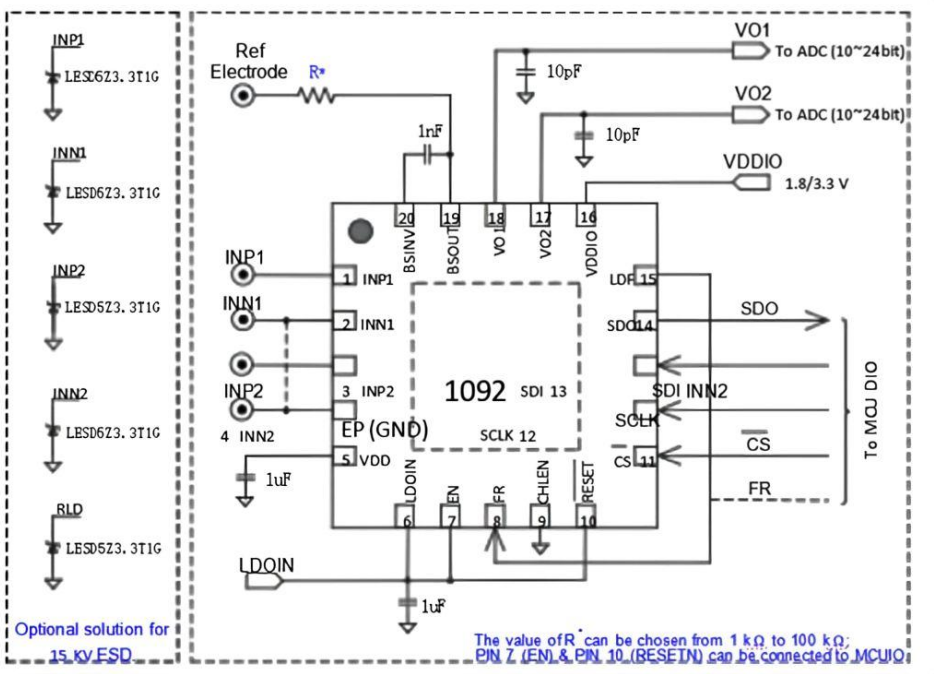


Figure 10. Dual-Channel Signal Conditioning with **4/5** Electrodes

## 6.2. RLD Electrode (Reference Electrode) Configuration

To improve the system CMRR performance, a driven lead (or reference electrode) is recommended to be implemented when the FS1091/FS1092 is adopted in practical applications. It is available through the bias

drive circuitry to minimize the effects of common-mode voltages induced by the power line and other interfering sources. As a safety measure, place a resistor between the output of the bias amplifier pin (PIN19: BSOUT) and the electrode connected to the subject to ensure that current flows in a limited range. For details, see the Theory of Operation Section (Bias Drive Circuitry).

For wearable EEG systems, the amplitude of the EEG signal is small. Additionally, the body movement of the subject creates large motion artifacts, and the long lead length makes the system susceptible to common-mode interference. A driven electrode is strongly recommended in this application to maintain high-quality signals, which can significantly improve the rejection of noise and motion artifacts.

What's important is that there is no strict requirement for the location of the driven electrode. It can be placed near one of the sense electrodes (either INP or INN), or far away from them. It's worth noting that the driven electrode must be isolated from each of the input electrodes, avoiding short connections.

## 6.3. Driving ADCs

The ability of FS 1091/FS1092 to drive capacitive loads makes it ideal for driving an ADC without an additional buffer. However, depending on the input architecture of the ADC, a simple, low-pass RC network may be required to decouple the transients from the switched capacitor input typical of modern ADCs. That can effectively reduce noise and aliasing. Therefore, the output pin of each signal channel (VO1: PIN18, VO2: PIN17) is recommended to be bypassed with a 10-pF capacitor in practical applications.

Definitely, a high-resolution ADC with a high effective number of bits (ENOB) is preferable to obtain high-quality EEG wave forms.

## 6.4. ESD Protection

The measured ESD rating for each pin of the FS1091/FS1092 is about ±4 kV for HBM mode and ±500 V for CDM mode. For further safety consideration, a complete solution includes further clamping to either supply using additional ESD devices, such as LESD5Z3.3T1G. In this case, the ESD rating of the system can achieve about 15 KV level.

## 6.5. Sensor Electrodes Material

The FS1091/FS1092 supports both wet-contact electrodes and dry-contact electrodes input for small biopotential recording. The sensor electrodes can be adopted are listed as follows,

- Wet electrodes: Silver-Silver Chloride (Ag-AgCl), etc.
- Dry electrodes: Metal (Cu, Ag), conductive fabric, graphene, etc.

EEG signal is pretty weak and prone to be interrupted by other noise and interference. Definitely, the use of wet electrodes can significantly enhance the interface contact between the electrodes and subject. Thus, low contact resistance can be obtained to improve the recorded signal quality.

## 6.6. PCB Layout Recommendations

Due to the weak biosignals, it is pretty important to follow good layout practices to optimize system performance.

### 6.6.1. Power Supplies and Grounding

The FS1091/FS1092 has a built-in LDO. VDD, as the output of the LDO, provides the supply for the entire integrated circuit, which should be as quiet as possible. For supply pins LDOIN and VDD, each pin should be

bypassed with a 1-µF capacitor. Alternatively, a decoupling circuit using a 1-µF capacitor in parallel with a 0.1-µF capacitor is also recommended. Place a 0.1-µF capacitor close to the supply pin. A 1-µF capacitor can be used farther away from the device. The placement of the digital circuits (such as the DSP, micro controllers, and FPGAs) in the system is done such that the return currents on those devices do not cross the FS1091/FS1092 analog return path. It is worth noting that excessive decoupling capacitance may increase power dissipation during power cycling.

### 6.6.2. Shielding Analog Signal Paths

As with any precision circuit, it is essential to keep the input traces symmetrical and length-matched and make wires short, direct interconnections and avoid stray wiring capacitance, particularly at the analog input pins. These analog input pins are high-impedance and extremely sensitive to extraneous noise. Digital signals should be kept as far as possible from the analog input signals on the PCB. What' s more, splitting the ground plane (Digital and Analog) on a mixed-signal PCB to isolate the digital circuits from analog circuits is recommended, which may significantly improve the noise rejection of the system.

# 7. Package Information

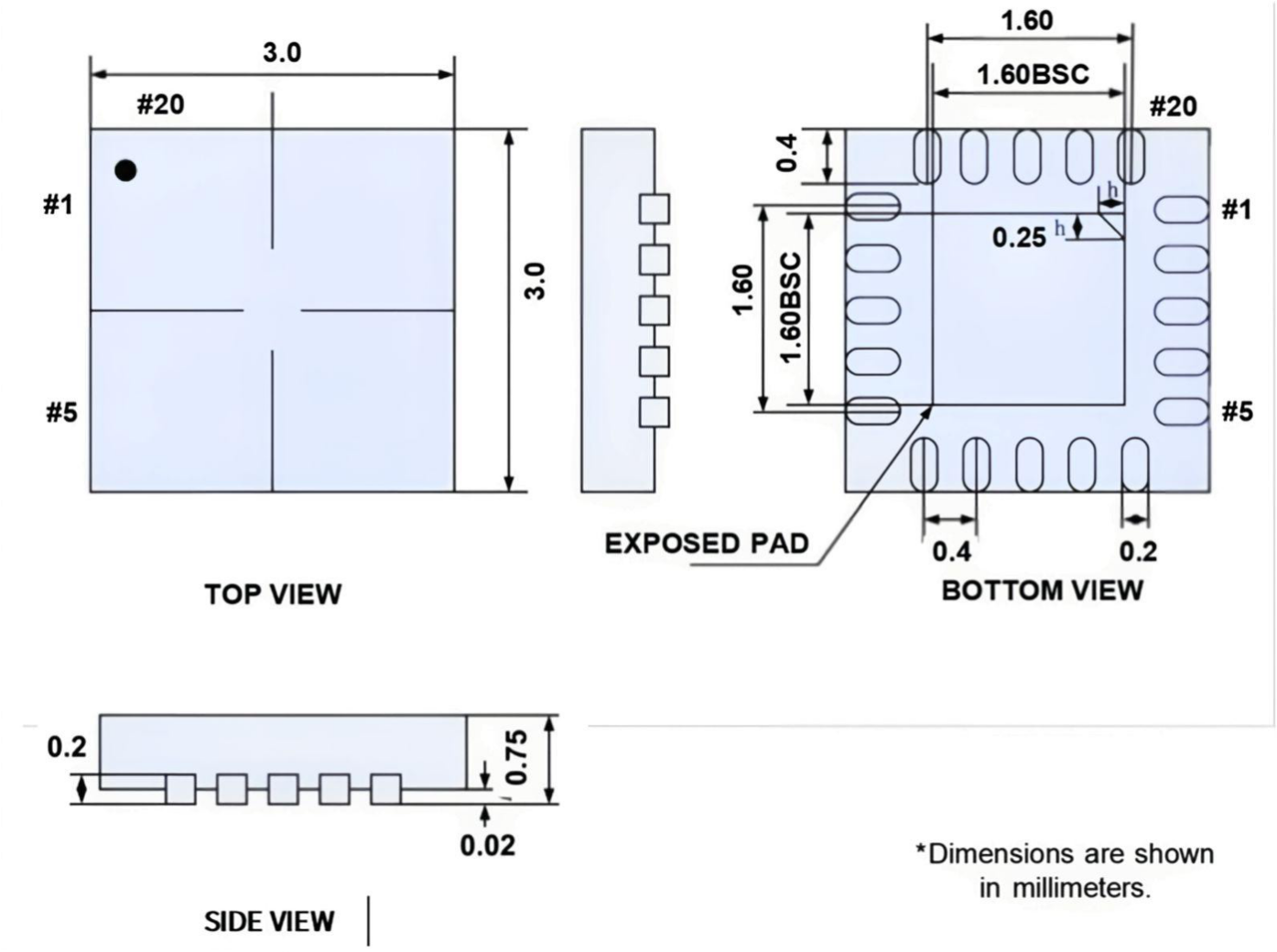


Figure 11. 20-Pin Quad Flat No-Lead Package.

## 7.1. NOTE for Exposed PAD:

This package incorporates an exposed pad that is designed for circuit ground and thermal heat sink. This pad **must** be soldered directly to the ground plane of the printed circuit board (PCB).

# 8. Ordering Guide

| Model | Device Name | Description | Size | Device Photo |
|---|---|---|---|---|
| FS1081/2 | ECG Chip | Single/Dual-channel analog front-end chip. | QFN-20 3×3mm |  |
| FS1091/2 | EEG Chip | Dual-channel analog front-end chip. | QFN-20 3×3 mm |  |



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